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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KEBEDE, BROOK	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/462,994	SCHWALKE ET AL.
	Examiner	Art Unit
	Brook Kebede	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on September 15, 2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claim 22 recites the limitation "a plurality of conductive filler that are arranged to **establish a uniform geometrical occupation** by the conductive useful structures and the conductive filler structures" in lines 3-5. However, the recited limitation does not have a support as the specification originally filed. Applicants are required to cancel the new matter in the reply to this Office Action.

Claim 24 recites the limitation " the conductive filler structures being arranged such that **a uniform geometrical occupation** by the conductive useful structures and the conductive filler structures is established" in lines 2-4. However, the recited limitation does not have a support as the specification originally filed. Applicants are required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 22 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 22 recites the limitation "a plurality of conductive filler that are arranged to **establish a uniform geometrical occupation** by the conductive useful structures and the conductive filler structures" in lines 3-5. However, the recited limitation does not have a support as the specification originally filed. Therefore, the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 24 recites the limitation " the conductive filler structures being arranged such that **a uniform geometrical occupation** by the conductive useful structures and the conductive filler structures is established" in lines 2-4. However, the recited limitation does not have a support as the specification originally filed. Therefore, the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action::

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects

for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 11, 15, 16, 18, and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirakawa et al. (US/4,590,508).

The rejection that was mailed on May 8, 2003 is maintained and repeated herein below as of record.

Re claims 11 and 22, Hirakawa et al. disclose an integrated circuit arrangement having at least one doped region (103-2) is provided in a semiconductor substrate (201); a plane arranged on a surface of the semiconductor substrate (201) having a number of conductive useful structures (104-1 104-2) and at least one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function (not labeled) (i.e., a dummy gate or resistor); and the conductive filler structure (not labeled) is conductively connected to the doped region and has uniform geometrical occupation (103-7) (see Figs. 1 - 10).

Re claim 15, as applied to one of the claims 11 above, Hirakawa et al. disclose all the claimed limitation including the limitation wherein the conductive useful structures (104-1 104-2) are gate electrodes; and wherein the conductive filler structure (not labeled) contains the material of the gate electrode (see Figs. 1 – 10).

Re claim 16, as applied to one of the claims 11 above, Hirakawa et al. disclose all the claimed limitation including the limitation whereby the doped region (103-7) is a doped well or the semiconductor substrate (10) (see Figs. 1 - 10).

Re claims 18, 23, and 24, Hirakawa et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (103-7) in a semiconductor substrate (201); forming a plane (not labeled) on a surface of the

semiconductor substrate (201) by applying a structuring a conductive useful structures (104-1 104-2) and at least one conductive filler structure (not labeled) producing an insulation layer (207) surrounding and covering the conductive useful structures (104-1 104-2) and the conductive filler structure (not labeled); and producing a conductive connection between the conductive filler structure (not labeled) and the doped region (103-7); including the limitation wherein conductive useful structures and the conductive filler structure exhibit essentially the same height and the conductive filler structure has not circuit orientated function and have uniform geometrical occupation (see Figs. 1-10).

Re claim 21, as applied to one of the claims 18 above, Hirakawa et al. disclose all the claimed limitation including the limitation whereby the doped region (103-7) is the semiconductor substrate (201) (see Figs. 1 - 10).

6. Claims 11 and 13-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimomura et al. (US/5,736,421).

The rejection that was mailed on May 8, 2003 is maintained and repeated herein below as of record.

Re claim 11, Shimomura et al. disclose an integrated circuit arrangement having at least one doped region (106) is provided in a semiconductor substrate (101); a plane arranged on a surface of the semiconductor substrate (101) having a number of conductive useful structures (113) and at least one conductive filler structure (112) (i.e., a dummy gate or resistor) which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function; and the conductive filler structure (112) is conductively connected to the doped region (106) (see Fig. 1).

Re claim 13, as applied to claim 11 above, Shimomura et al. disclose all the claimed limitation including the limitation a contact (not labeled) connecting the conductive filler structure (112) to the doped region (106) via a via hole (not labeled) (see Fig. 1).

Re claim 14, as applied to claim 13 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein said through hole (not labeled) overlaps said conductive filler structure (112) and said doped region (106) exposing surface of the said conductive filler structure (112) and said a surface of said doped region (106), said contact (not labeled) being in communication with said conductive filler structure (112) and said surface of the doped region (106) (see Fig. 1).

Re claim 15, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein the conductive useful structures (113) are gate electrodes; and wherein the conductive filler structure (112) contains the material of the gate electrode (i.e., polysilicon, see Col. 7, line 61 – Col. 8, line 26) (see Fig. 1).

Re claim 16, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation whereby the doped region (106) is a doped well or the semiconductor substrate (101) (see Fig. 1).

Re claim 17, as applied to on of the claims 16 above, Uchara et al. disclose all the claimed limitation including the limitation a metallization layer (not labeled) is arranged above the plane wherein the conductive filler structure (112) is arranged; and a further contact connecting the conductive filler structure (112) and the metallization layer (not labeled) (see Fig. 1)

Re claim 18, Shimomura et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (106) in a semiconductor substrate (101); forming a plane (not labeled) on a surface of the semiconductor substrate (101) by applying a structuring a conductive useful structures (113) and at least one conductive filler structure (112) producing an insulation layer (106) surrounding and covering the conductive useful structures (113) and the conductive filler structure (112); and producing a conductive connection between the conductive filler structure (112) and the doped region (106) (see Fig. 6-9(e)).

Re claim 19, as applied to claim 18 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein said steps of producing connection between said conductive filler structure (112) and said doped region (106) further comprsing steps of: opening a through hole (not labeled) in said insulation layer (106), said though hole (not labeled) respectively partially overlapping said conductive filler structure (112) and said the doped region (106) for partially uncovering a surface of said doped region (106) and surface of said conductive filler structure (112); and forming a contact (not labeled) through hole (not labeled), said contact (not labeled) being in communication with said surface of said conductive filler structure (112) and said surface of said doped region (106) (see Fig. 1)

Re claim 20, as applied to claim 18 above, Shimomura et al. disclose all the claimed limitations including producing a metallization layer (not labeled) above the plane wherein the conductive filler structure (113) is formed; producing a further contact (not labeled) connecting the conductive filler structure (112) connecting to the metallization layer (not labeled) (see Fig. 1).

Re claim 21, as applied to one of the claims 11 above, Shimomura et al. disclose all the claimed limitation including the limitation whereby the doped region (106) is the semiconductor substrate (101) (see Fig. 1).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimomura et al. (US/5,736,421) in view of Uehara et al. (US/5,698,902).

The rejection that was mailed on May 8, 2003 is maintained and repeated herein below as of record.

Re claim 12, as applied to claim 11 above, Shimomura et al. disclose all the claimed limitation including the limitation a planarizing insulation layer (106) surrounding the conductive useful structures (113) (see Fig. 1).

However, Shimomura et al. do not specifically disclose wherein the conductive useful structures (113) and the conductive filler structure (112) exhibit essentially the same height.

Uehara et al. disclose integrated circuit arrangement having at least one doped region (21) is provided in a semiconductor substrate (10); a plane arranged on a surface of the semiconductor substrate (10) having a number of conductive useful structures (50a) and at least one conductive filler structure (50b); and wherein the conductive useful structures (50a) and the conductive filler structure (50b) exhibit essentially the same height (see Fig. 6). Uehara et al. also disclose that "he lower films of the dummy electrodes (i.e., conductive filler structure) are formed flush with the isolation and in contact with the side edges of the isolation. With the dummy electrodes (i.e., conductive filler structure), any gate electrode (i.e., conductive useful structure) can be formed in a line-and-space pattern (i.e., exhibiting essentially same height), so that the finished sizes of the gate electrode become uniform. This enables a reduction in gate length and therefore provides a semiconductor device of higher integration which is operable at a higher speed and substantially free from variations in finished size resulting from the use of different gate patterns." (see the abstract). Hence one of ordinary skill in the would have motivated to arrange the conductive useful structures and the conductive filler structure exhibit essentially the same height in order to make a uniform finished sizes of the gate electrode.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided Shimomura et al. reference with arranging the conductive useful structures and the conductive filler

structure to exhibit essentially the same height as taught Uehara et al. because the arrangement would have provided the semiconductor device to have a uniform finished sizes of the gate electrode.

Response to Arguments

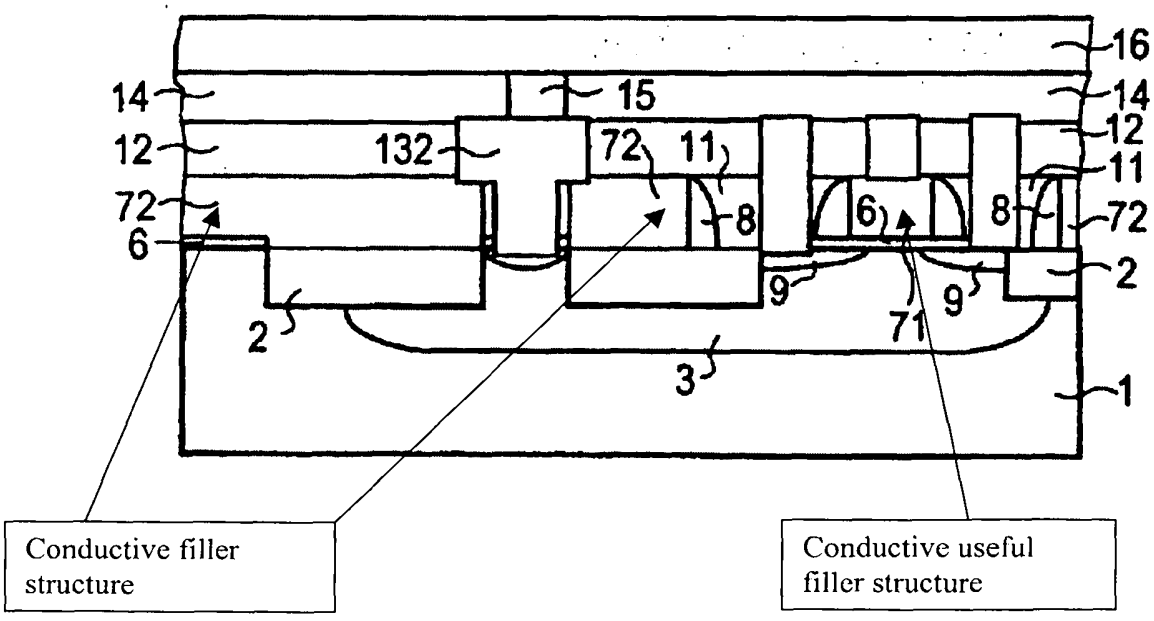
9. Applicants' arguments filed on September 15, 2003 have been fully considered but they are not persuasive.

With respect to claims rejection, i.e., Claims 11, 15, 16, 18 and 21, under 35 U.S.C 102(b), applicants argued that "Hirakawa fails to disclose the use of filler structures that perform no circuit-oriented functions, as claimed by amended claim 11 Furthermore, Hirakawa fails to disclose (claim 18) useful structures and conductive filler structure formed on a plane. Applicants have amended claim 11 to include two additional features: a) the conductive useful structures and the conductive filler structure exhibit essentially the same height, and b) the conductive filler structure has no circuit oriented function . . . Hirakawa fails to disclose that both the useful structure 104-1 and the "dummy filler structure" on the right side of Figure 4 (without reference number) are formed by applying and patterning one and the same conductive layer...Applicants do not believe that present claim 18 needs to be amended because it includes the feature (in the second method step) that the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer. This implicitly includes the feature that these kinds of structures have the same height."

In response to the applicants argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above.

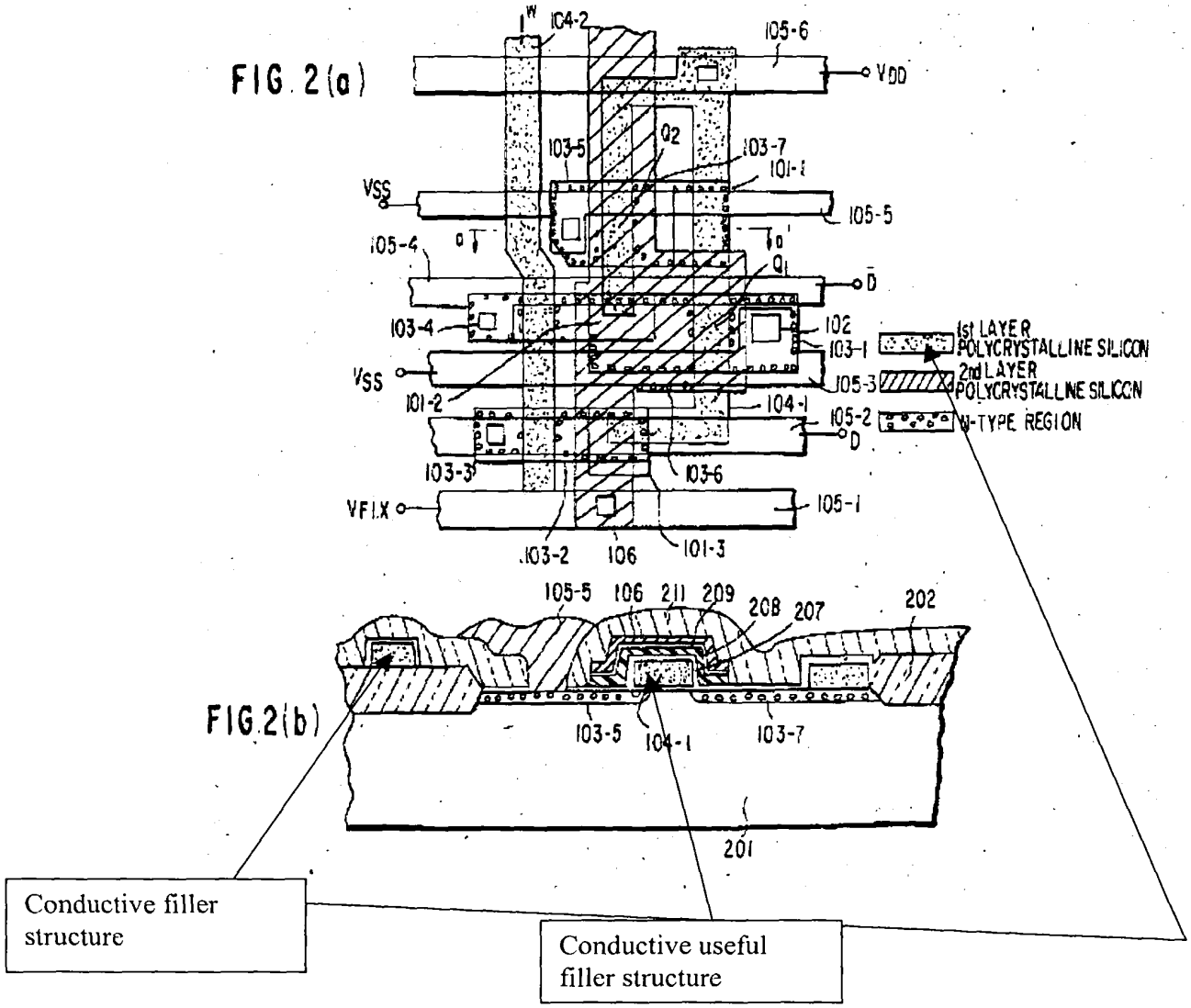
Prior responding applicants' contention that Hirakawa fails to disclose the use of filler structures that perform no circuit-oriented functions, as amended in claim 11, the Examiner respectfully submits the instant application drawing Fig. 7 herein below to show inconsistency between what is being claimed and what is applicants presented to support their argument to show what Hirakawa et al. '508 patent teach or does not teach.

FIG 7



As shown above in Fig. 7, i.e., the instant application drawing, the conductive useful structure **71** formed over the gate oxide film **6**. In the other hand, the conductive filler structure **72** formed on the STI **2** (shallow trench isolation) that is planar with the substrate **1.** As Fig. 7 shows, the conductive filler structure **72** does not have same height as the conductive useful structure **71.** As depicted on Fig. 7, one of ordinary skill in the art will conclude that the height of **72** is not equal to the height of **71.** In contrary applicants assertion, the **height of 72** equals to the **height of 71** plus **height of 6.**

In response to applicants argument that Hirakawa fails to disclose "one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function," the Examiner respectfully submits that Hirakawa et al. '508 disclose all the claimed limitations in including the limitation one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function. The Examiner respectfully would like to point out to Figs. 2(a) and 2(b) of Hirakawa et al. '508 as shown herein below.



As shown in Fig. 2(a), the first layer polysilicon layer, i.e., the conformal layer used to form the dummy gate (not labeled) (conductive filler structure) and the gate **104-1** (conductive useful structure) basically formed same polysilicon layer which later patterned and they essentially exhibit same height. In addition, the conductive filler

structure, as shown in Figs. 2(a) and 2(b), has no circuit - oriented function. Furthermore, the rejected claim, i.e., claim 11, does not claim that "the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer" as applicants argued. Hence applicants' argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore the rejection, i.e., Claims 11, 15, 16, 18 and 21, under 35 U.S.C 102(b) is deemed proper.

With respect to claims rejection, i.e., Claims 11 and 13-21, under 35 U.S.C 102(e), applicants argued that "Shimomura fails to disclose the elements of amended independent claim 11 and independent claim 18 that the filler structure and useful

structures 10 have essentially the same height or are formed by applying and patterning the same conductive layer. According to amended claim 11, and existing claim 18 (as noted previously) Shimomura fails to disclose that structure 112 in Figure 1 regarded as filler structure in the Office Action and the conductive useful structure 113 have essentially the same height (they are not made of the same number of layers). Furthermore, the structure 112 is a resistor and accordingly has a circuit-oriented function, in contrast with claim 11, as amended. As to method claim 18, Shimomura fails to disclose that both structures 112 and 113 are formed by applying and patterning one and the same conductive layer..."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Shimomura et al. '421 disclose all the claimed limitation as applied herein above. In addition, Shimomura et al. also disclose including the limitation one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function.

Furthermore, the rejected claim, i.e., claim 11, does not claim that "the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer" as applicants argued. Therefore, applicants' argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer) are not recited

in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore the rejection, i.e., Claims 11 and 13-21 under 35 U.S.C 102(e) is deemed proper.

With respect to claim rejection, i.e., Claim 12, under 35 U.S.C 103, applicants argued that "...the amended claim language distinguishes over prior art..."

In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits the combination of Shimomura et al. '421 and Uehara et al. '902 teach all the claimed limitation. In addition, the Examiner respectfully would like to point out that "conductive filler structure" and "conductive useful structure" has no any special meaning as one of ordinary skill understands in light of the instant application disclosure and Figures 1-7, as particularly shown in Fig. 7 herein above. The "conductive filler structure **72**" is a resistor and the "conductive useful structure **71**" is a gate electrode. If there is a different interpretation can be made as alleged by applicants, applicants should provide the Office an evidence that conductive

filler structure **72** has different function than form being resistor and conductive useful structure **71** also being gate electrode. What is the "conductive useful structure" mean? What is the "conductive filler structure" mean? Applicants need to clarify this matter because their argument suggest otherwise (see Applicants argument in Pages 10-12) and the whole application may be rejected under 35 U.S.C. 112 first and second Paragraph for lack of enabling disclosure and lack of clarity.

Therefore, the *prima facie* case of obviousness has been met and the rejection under 35 U.S.C. § 103 is deemed proper.

Conclusion

10. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
November 11, 2003

W. DAVID COLEMAN
PRIMARY EXAMINER